

Notice of References Cited

Application/Control No.

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Applicant(s)/Patent Under
Reexamination
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Examiner

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Art Unit

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	W	Rodrigues-Henriquez, F. et al. "4.2 Gbit/s single-chip FPGA implementation of AES algorithm," received 2 April 2003 for Electronics Letters Vol. 39 No. 15, 24 July 2003, pp. 1115-1116.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.